REMARKS

Claims 1-26 and 51-85 are now pending in the application. Applicants cancel claims 27-50 without disclaimer or prejudice to the subject matter contained therein. Applicants thank the Examiner for the courtesy extended during the personal interview conducted on June 28, 2006. During the interview, Applicants' representative and the Examiner discussed the Examiner's interpretation of the Jaggar reference. No agreement was reached. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

DOUBLE PATENTING

Claims 1, 11-14, 24-26, 51, 61, 64, 74, 78, and 80 are provisionally rejected under the judicially created doctrine of double patenting over claims 1 and 5-7 of copending Patent Application No. 10/627,269. Applicants include herewith a terminal disclaimer.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-11, 14-24, 57-58 and 60-85 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Jaggar (U.S. Pat. No. 5,701,493). This rejection is respectfully traversed.

With respect to claim 1, Jaggar fails to show, teach, or suggest a register file for a data processing system comprising an unbanked memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode.

Instead, as best understood by Applicants, Jaggar discloses a banked register structure.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Jaggar fails to disclose the limitation of an unbanked memory unit having a plurality of memory locations addressable by an encoded address.

As shown in prior art FIG. 1 of the present application, conventional microprocessor architectures include a "banked register" structure. For example, a microprocessor accesses general purpose registers 100 in a normal mode, and accesses banked registers 102 in an interrupt mode. The banked registers 102 are located in a separate memory unit. In other words, "in the interrupt mode, different registers in a separate memory unit, i.e., banked registers, are accessed than in the normal mode." (Paragraph [003]).

In contrast, the present invention is directed to an unbanked memory unit instead of "separate memory units such as "banked registers."" (Paragraph [034]). For example, as shown in an exemplary embodiment in FIGS. 4 and 5, a register file memory unit 400 is unbanked, and instead includes a plurality of memory locations addressable by encoded addresses. In other words, the encoded addresses all address memory locations in the same unbanked memory unit (i.e. the register file

memory unit 400) as opposed to addressing memory locations in separate memory units as shown in FIG. 1.

As best understood by Applicants, Jaggar is absent of any teaching or suggestion of an unbanked memory unit that includes a plurality of memory locations addressable by encoded addresses, and instead is directed to a banked architecture that accesses banked registers in separate memory units as shown in Applicants' prior art FIG. 1. For example, FIG. 1 of Jaggar includes a register bank 16. A particular register in the register bank is addressed based in part on contents of a bank of saved processing status registers 20. In other words, the register bank 16 appears to represent a banked memory architecture.

FIGS. 2 and 9 of Jaggar disclose the banked memory architecture in further detail. For example, FIG. 9 appears to disclose different banks of registers for User32, System, FiQ32, SVC32, Abt32, IRQ32, and Undef32 modes as shown below:

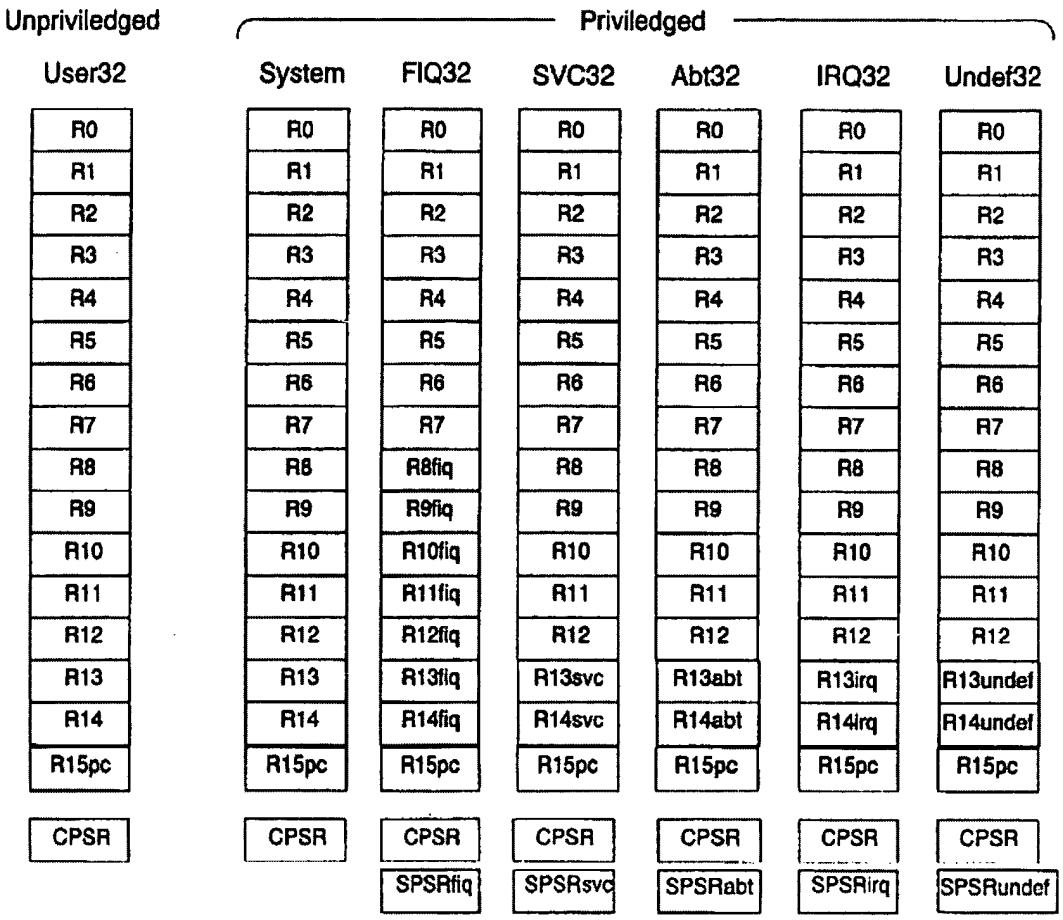

Fig.9

Applicants respectfully note that the banked memory architecture shown in FIGS. 2 and 9 of Jaggar appears to be analogous to the banked structure shown in Applicants' prior art FIG. 1. Applicants respectfully submit that the present invention is directed to an unbanked memory unit as claim 1 recites and that Jaggar appears to be absent of any teaching or suggestion of such a structure. Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. The remaining claims should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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